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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,970	06/25/2001	Adrian E. Ong	M-9820 US	1405
75	90 07/13/2005		EXAM	INER
Philip W. Woo			CHANG, DANIEL D	
Sidley Austin B	rown & Wood LLP			
555 California Street			ART UNIT	PAPER NUMBER
Suite 5000			2819	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<u>+'B</u>		
	Application No.	Applicant(s)
Office Assistant Commencer	09/888,970	ONG, ADRIAN E.
Office Action Summary	Examiner	Art Unit
TL- MAU NO DATE ALL:	Daniel D. Chang	2819
The MAILING DATE of this communication Period for Reply	ion appears on the cover sheet wit	n tne correspondence address
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNICATOR - Extensions of time may be available under the provisions of 37 after SIX (6) MONTHS from the mailing date of this communicator if the period for reply specified above is less than thirty (30) dayor if NO period for reply is specified above, the maximum statutor Failure to reply within the set or extended period for reply will, any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	TION. CFR 1.136(a). In no event, however, may a reation. ys, a reply within the statutory minimum of thirty y period will apply and will expire SIX (6) MONT by statute, cause the application to become ABA	ply be timely filed (30) days will be considered timely. THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).
Status		
 1) Responsive to communication(s) filed on 2a) This action is FINAL. 2b) Since this application is in condition for a closed in accordance with the practice up 	This action is non-final. Allowance except for formal matte	•
Disposition of Claims		
4) ☐ Claim(s) 1-24 is/are pending in the applitude 4a) Of the above claim(s) is/are well 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-24 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction	rithdrawn from consideration.	
Application Papers		
9)☐ The specification is objected to by the Ex 10)☒ The drawing(s) filed on 25 June 2001 is/s Applicant may not request that any objection Replacement drawing sheet(s) including the 11)☐ The oath or declaration is objected to by	are: a)⊠ accepted or b)⊡ object to the drawing(s) be held in abeyand correction is required if the drawing(s)	ce. See 37 CFR 1.85(a). s) is objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119		
12) Acknowledgment is made of a claim for f a) All b) Some * c) None of: 1. Certified copies of the priority doc 2. Certified copies of the priority doc 3. Copies of the certified copies of the application from the International * * See the attached detailed Office action for	uments have been received. uments have been received in Ap ne priority documents have been of Bureau (PCT Rule 17.2(a)).	oplication No received in this National Stage
Attachment(s) 1) Notice of References Cited (PTO-892)		ummary (PTO-413)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-9 3) Information Disclosure Statement(s) (PTO-1449 or PTO- 		/Mail Date formal Patent Application (PTO-152)
Paper No(s)/Mail Date	6) Other:	

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Acknowledgement

Receipt is acknowledged of the Amendment filed June 29, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Balamurugan et al. (US 6,320,795 B1, "Balamurugan", hereinafter).

Regarding claim 14, Balamurugan discloses, in Figs. 1 and 2, a system for driving a data signal, comprising:

a plurality of bit lines (16 lines connecting 14 from each of the cells 10; see col. 2, lines 39+);

a data bus (14) having a plurality of bus lines (it is inherent that a data bus have a plurality of bus lines), wherein each bus line is connectable (by 42) to a respective portion of the plurality of bit lines;

a charging circuit (16) coupled to at least one of the bus lines of the data bus, wherein the charging circuit is configured to pre-charge (20) the at least one of the bus lines of the data bus (line 14) to a first voltage level (18) in advance of driving a first type of data signal (data signal

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from first register file cell 10 or 40) or a second type of data signal (data signal from second register file cell 10 or 40) across the at least one of the bus lines.

Regarding claim 15, Balamurugan discloses, in Fig. 1 a keeper circuit (24) coupled to the at least one of the bus lines of the data bus, wherein the keeper circuit is configured to maintain the at least one of the bus lines of the data bus at the first voltage level after the at least one of the bus lines of the data bus has been charged.

Regarding claim 16, Balamurugan discloses, in Fig. 2 that the pull-down circuit comprises:

a transistor (42) coupled at one end to the at least one of the bus lines of the data bus and at the other end to ground;

logic circuitry (44) coupled to a gate of the transistor, wherein an output signal from the logic circuitry controls the transistor.

Regarding claim 17, Balamurugan discloses, in Fig. 2 that the logic circuitry comprises a first input terminal (48) for receiving an equilibration signal and a second input terminal (50) for receiving a data signal.

Regarding claim 18, Balamurugan discloses, in Fig. 2 that the logic circuitry comprises a NOR gate (44).

Regarding claim 19, Balamurugan discloses, in Fig. 2 that the charging circuit comprises: a transistor (16) coupled at one end to a power supply voltage source and at the other end to the at least one of the bus lines of the data bus, wherein the transistor is controlled by an equilibration signal (20).

Regarding claim 20, Balamurugan discloses, in Fig. 1 the keeper circuit comprises:

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a transistor (26) coupled at one end to a power supply voltage source and at the other end to the at least one of the bus lines of the data bus; and

logic circuitry (28) coupled to a gate of the transistor, wherein an output signal from the logic circuitry controls the transistor.

Regarding claim 21, Balamurugan discloses, in Fig. 1 the logic circuitry comprises an inverter gate (28).

Regarding claim 24, Balamurugan discloses, in Fig. 1, a pull-down circuit (30, 32 in Fig. 1; 42 in Fig. 2) coupled to the at least one of the bus lines of the data bus (line 14), wherein the pull-down circuit is configured to pull the at least one of the bus lines of the data bus to a second voltage level (36).

Method claims 1-2, 4-13, 22, and 23 are essentially the same in scope as apparatus claims 14-21 and 24 and are rejected similarly.

Regarding claim 3, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments filed March 7, 2005 have been fully considered but they are not persuasive.

Applicant argues, on page 8 of the amendment filed June 29, 2005, that Claim 1, as amended, recites *inter alia*, "'pre-charging at least one of the bus lines of the data bus to a first voltage level in advance of driving a first type of data signal or a second type of data signal

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across the at least one of the bus lines.' Balamurugan et al. does not disclose such limitation. As such, this reference does not anticipate Applicant's invention recited in Claim 1." and "Claim 14, as amended, recites *inter alia*, 'a charging circuit coupled to at least one of the bus lines of the data bus, wherein the charging circuit is configured to pre-charge the at least one of the bus lines of the data bus to a first voltage level in advance of driving a first type of data signal or a second type of data signal across the at least one of the bus lines.' Balamurugan et al. does not disclose such limitation. As such, this reference does not anticipate Applicant's invention recited in Claim 14.'".

Balamurugan et al. discloses that line 14 is a bit line. However, line 14 can be interpreted as one of a plurality of bus lines and lines connecting from register file cell 10 or 40 to line 14 can be called bit lines (x16). It is noted that "the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art," *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997). Therefore, a charging circuit (16) is coupled to at least one of the bus lines (14) of the data bus, wherein the charging circuit is configured to pre-charge (20) the at least one of the bus lines (line 14) of the data bus to a first voltage level (18) in advance of driving a first type of data signal (data signal from first register file cell 10 or 40) or a second type of data signal (data signal from second register file cell 10 or 40) across the at least one of the bus lines, as set forth in claim 14 and similarly with claim 1.

Balamurugan et al. teaches all the elements and means of the claimed invention of the claims 1-24 as discussed above and the rejection is maintained.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang Primary Examiner

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DANIEL CHANG PRIMARY EXAMINER